Improved Method for Characterizing and Modeling Gigabit Flex-Circuit Based Interconnects

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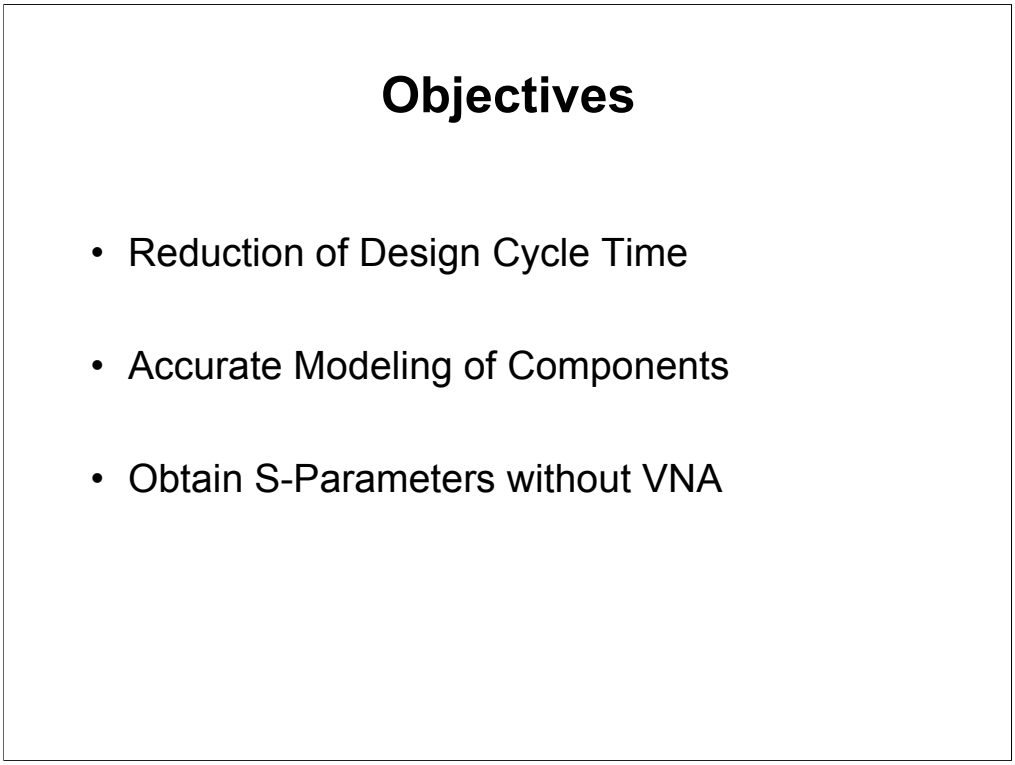
1.0 Introduction

This paper describes sophisticated, time-domain methods of accurately predicting time- and frequency-domain high-speed signal characteristics. The methods used are applied to a relatively new class of connectors whose flexible substrate allow them to take advantage of these predictive procedures. The measurement process is based on well known Time Domain Reflectometer (TDR) theory. However, additional numerical tools are applied to create several frequency-domain characteristics that typically require a Vector Network Analyzer (VNA). This technique will be shown to characterize flexible interconnects, but other more traditional interconnects can be evaluated in the same fashion.

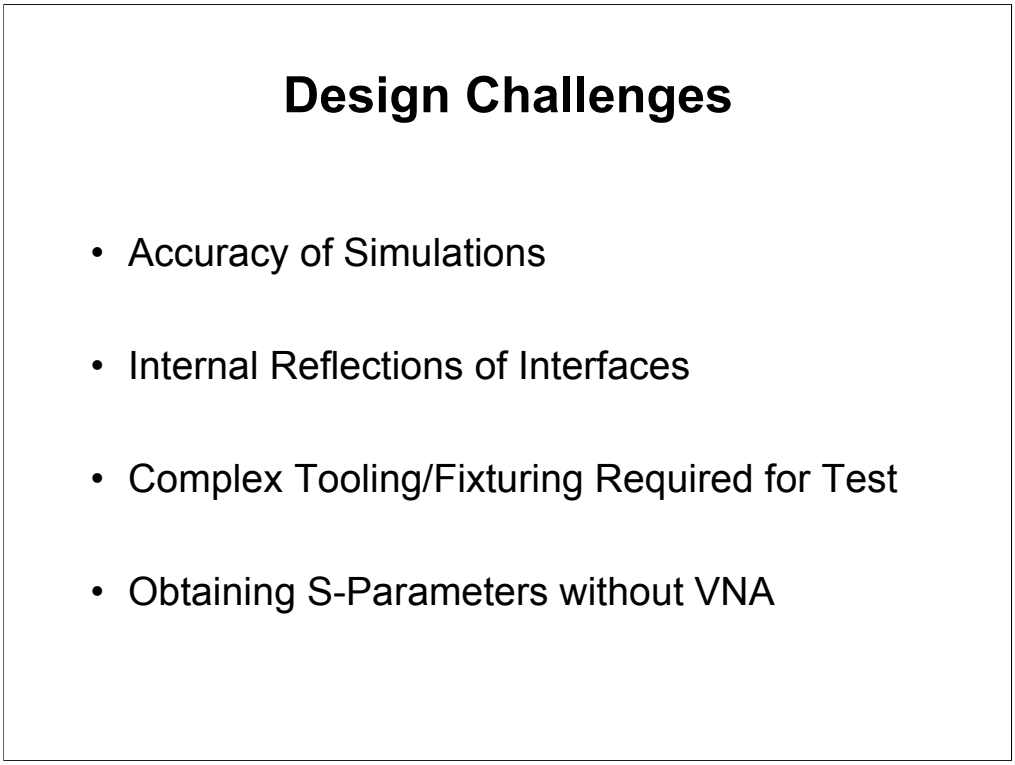


1.1 Objective

Reduction of design cycle time would be possible if the designer could quickly predict interconnect performance. Performance prediction is imperative to achieving a robust design in the required time to market.

The risetime of today's high speed digital signal transitions require analysis of interconnects as transmission lines. The FPC Interconnect has many discrete components which must be modeled separately. From the SMA to the PCB board trace, to the interface and the flexible circuit, each of these components must be accurately modeled.

Obtaining frequency domain characteristics such as S-Parameters are most often achieved by utilizing a VNA. If digital designers apply current simulation tools coupled with an intuitive instrument such as a TDR, they can now characterize the physical layer accurately and quickly.

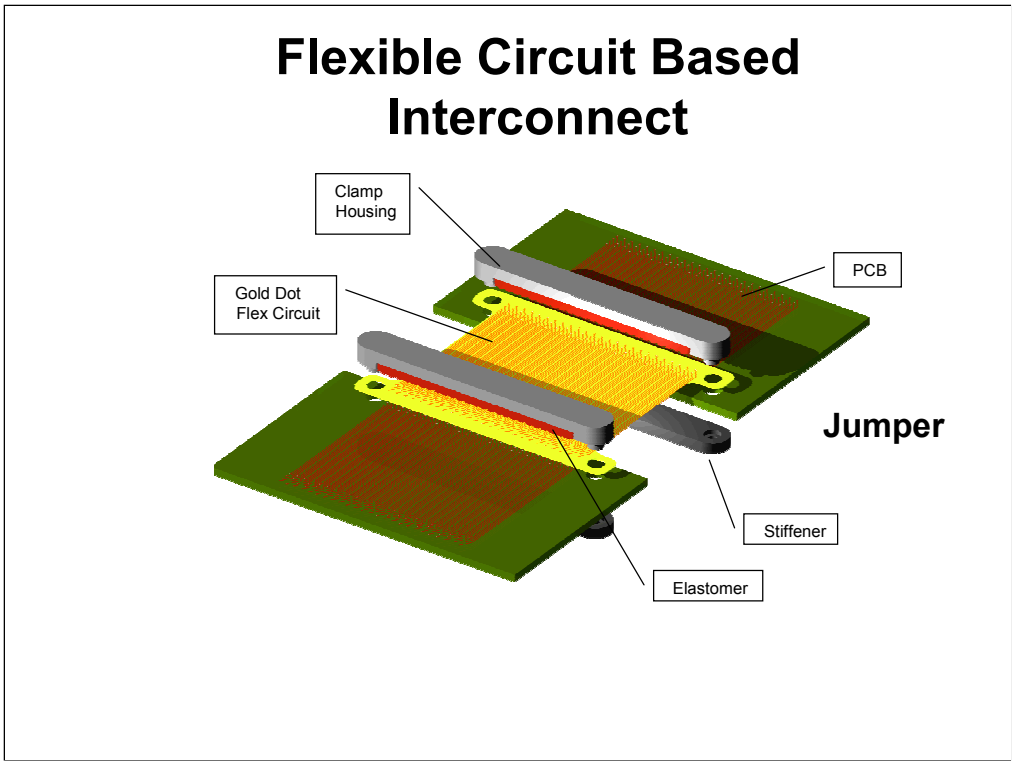


1.2 Design Challenges

Each interconnect component contributes a transition by which the signal can be degraded. Therefore, characterization and simulation must describe each and every impedance transition. These impedance discontinuities need to modeled and simulated accurately so that the electrical performance of the interconnect system can be predicted to prevent many design iterations.

Test fixturing for the flexible circuit is defined as the rigid printed circuit board with SMA connectors and the cables interfaced to the TDR. The test fixture may take longer to design and manufacture than the flexible circuit itself. Additionally, the tooling or fixturing often contributes to masking true impedance, making accurate measurements difficult to achieve. Quick, accurate performance predictions are necessary at the operating system rise time.

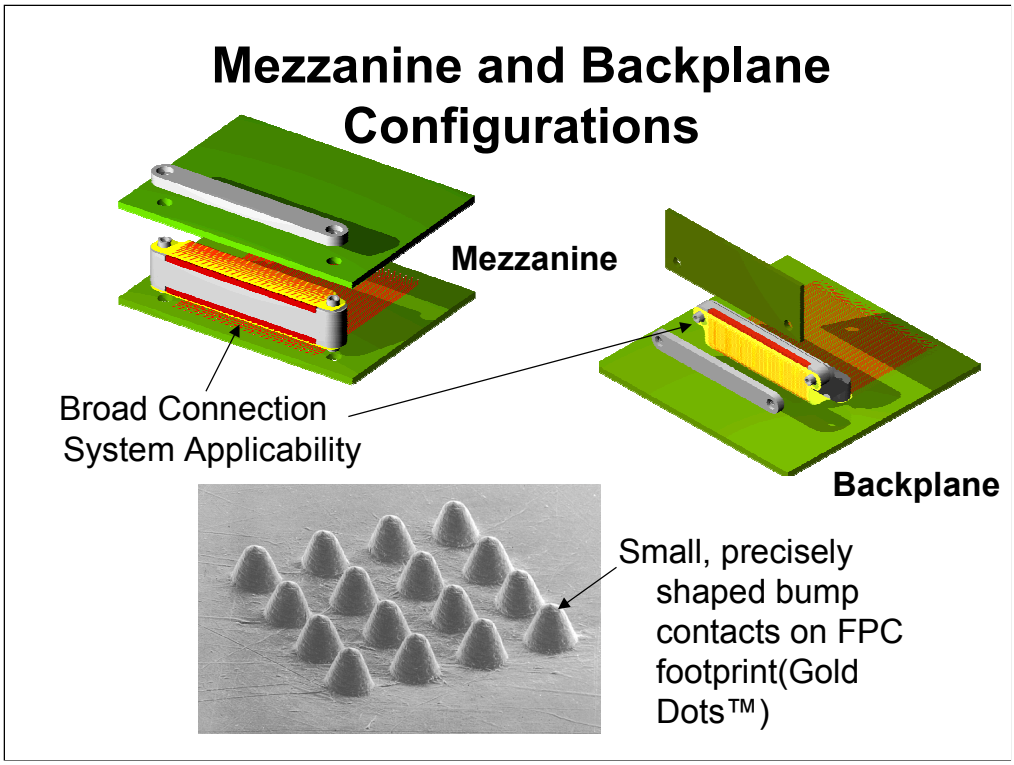
Time domain measurements to obtain characteristics such as impedance and crosstalk are easily and quickly obtained with TDR instrumentation. SPICE models and S-parameters are often required to fully characterize an interconnect. To achieve a multi-domain understanding of the physical layer, a software tool can be used to translate from the time domain to the frequency domain.



1.3 Flexible Circuit Interconnects

Flexible Circuit Interconnect based systems are preferred in special applications of high speed electrical connections between printed circuit boards (PCB's). These applications include PDA's, cell phones, and flat panel displays. A burgeoning field today for board to board flexible interconnects is high speed routers and switches. New switch fabric architectures such as InfiniBand™ will require flexible interconnect at data rates of 2.5 Gbps and risetimes of 100 picoseconds. High signal integrity will need to be designed into these interconnect devices to sustain such switching speeds.

As can be seen above, the flexible interconnects are typically configured as a simple mechanical compression device and a flex circuit.



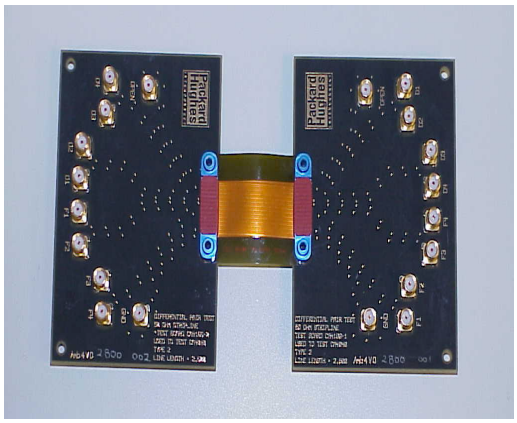
With the flexible circuit core, reforming the system into various configurations is a straightforward process as shown by the mezzanine and backplane configurations.

The flexible circuit carries the electrical signal from board to board, while the mechanical compression device, or clamp, provides the force between exposed pads on the FPC and PCB required to make reliable electrical connection.

Often the FPC may have a bump contact or Gold Dot to insure an interface that is mechanically robust and produces low signal reflections at the FPC to PCB interface.

Device Under Test
Gold Dot Flexible Printed Circuit (FPC)

- Differential Pair FPC Interconnect
  - Jumper
  - 52 Way
- FPC Configuration
  - .0032” Linewidth
  - .0089” Pitch within Differential Pair
  - .0230” Pitch Differential Pair to Differential Pair

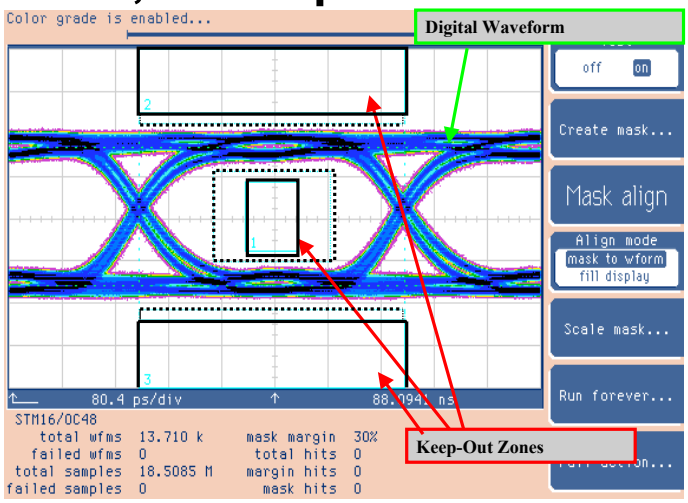


The FPC connector under test is a 52 way differential pair interconnect. This interconnect is comprised of 26 differential pairs. Each differential pair is separated by a ground. Two traces within the differential pair are separated by .0089 inches. Each trace is approximately .0032 inches wide (linewidth) and .0013 inches thick. The pitch from differential pair to differential pair was .023 inches. For this microstrip construction, the signal lines were approximately .0017 inches from the ground plane. The dimensions of these precisely manufactured components have a tremendous impact on the electrical performance of the interconnect.

Though a jumper Gold Dot FPC interconnect was tested, the interconnect possesses the electrical characteristics such as impedance and crosstalk much like the FPC mezzanine and backplane interconnect.

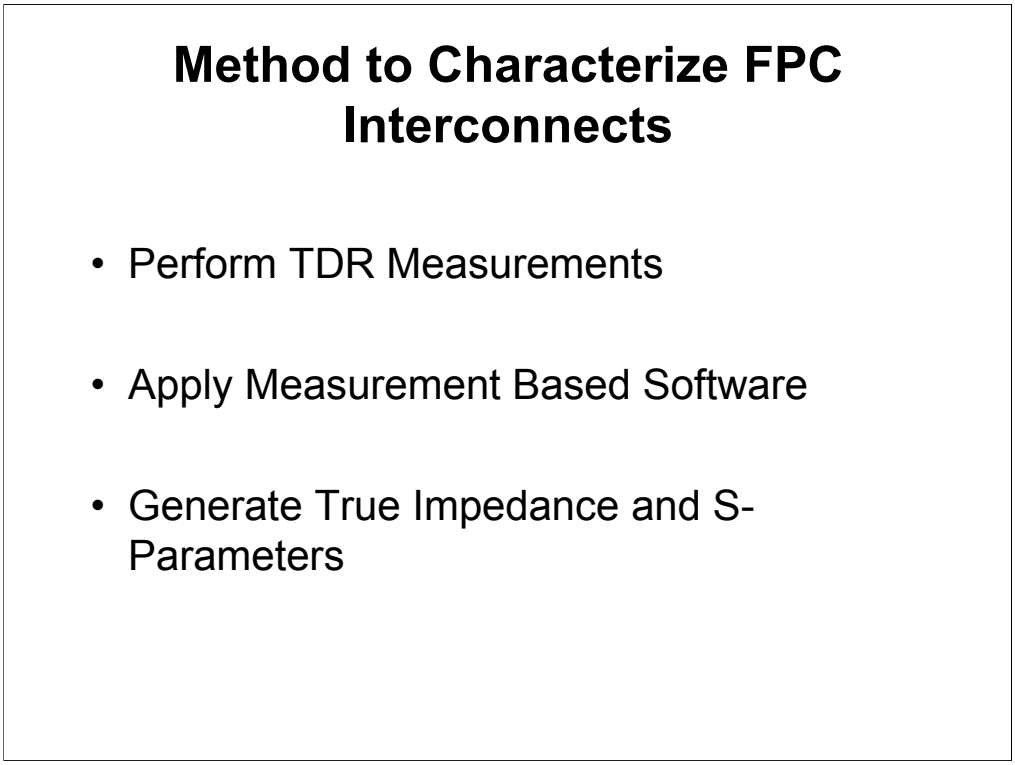
Eye Diagram Analysis
OC-48, 2.5 Gbps Mask

- OC-48 Keep Out Zones shown as Solid Red Frames
- Actual Performance shown as Dotted Red Frames
- Compliance with +30% Margin



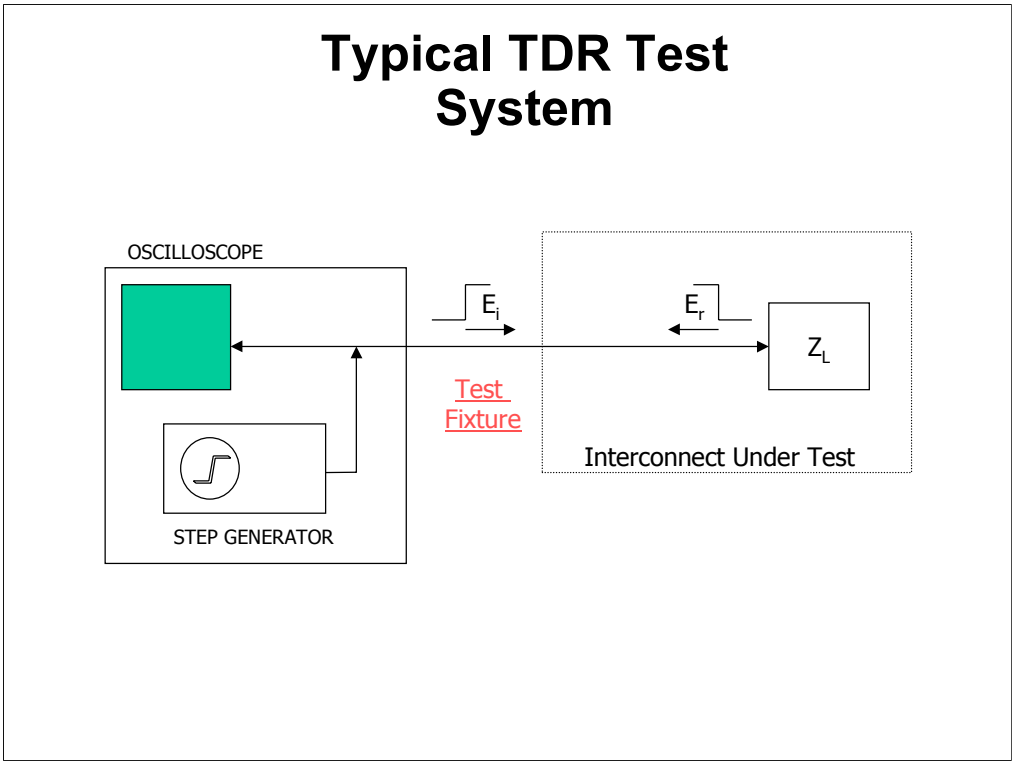
Because the FPC is built using PCB-like materials and processes, it can be characterized as a simple extension of the PCB. High performance has been documented for this class of connectors at 2.5 Gbps. (OC-48 class transmission[1].)

The performance of the basic microstrip and/or stripline structures across several measurements such as near end crosstalk, far end crosstalk, and attenuation can be predicted from classic texts and 2-D numerical analysis [2]. The challenging design issues arise in the contact zones, or footprint, of the connector where line spacing, via size, shape, and location, and grid definition become variable factors in the signal integrity equation. This experiment was performed with the following objective: develop advanced measurement and modeling techniques that would allow extended performance of flexible circuit interconnects into the Gbps range.



2.0 Improved Method to Characterize Using Time Domain Measurements and Simulation

An improved method to characterize interconnects was applied in order to decrease the design cycle time, while accurately measuring and predicting performance. For this method, measurement based software utilizes both the even and odd mode impedances of differential signal lines to enhance TDR measurements of the device.

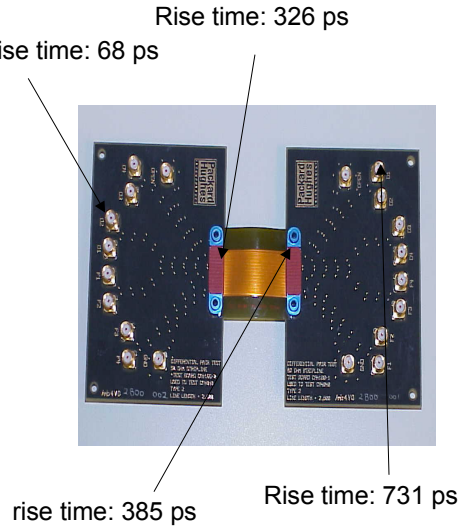


2.1 Time Domain Reflectometry

Time Domain Reflectometry(TDR) is a method that utilizes a high speed-digitizing oscilloscope with a built in step generator capable of launching a fast edge into a device under test (DUT). By monitoring the reflected wave from various impedance discontinuities encountered in the DUT, many characteristics of the device can be analyzed[3]. Whether or not a passive component adds excess inductance or excess capacitance to the circuit is of primary concern. Due to the high-speed signals on the IEEE 1394 physical layer, great care must be used when designing even the simplest passive components. Cables, connectors, printed circuit board traces, and chip packages can degrade signal integrity. Once this happens, all sorts of problems begin to occur. Crosstalk, reflections, glitches, logic errors, clock skew are just a few examples which can create havoc for the high-speed digital designer. The TDR technique highlights these unwanted signal reflections and allows improvement of signal integrity.

Rise time Degradation Due to Test Fixture

- **Bandwidth of test fixture is critical**
  - Allows Accurate Characterization
  - Higher Signal Integrity Analysis
- **Less bandwidth degrades TDR step rise time**
  - τ_r = 0.35/Bandwidth
- **Bandwidth limits data rate**



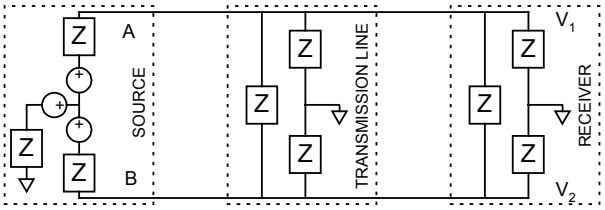
As the signals travel down the transmission lines, characteristics of the signals, such as rise time, may degrade. A simple way to determine degradation of signals is the application of time domain reflectometry. A TDR sends out a signal with a fast rise time step (typically 40 ps with 200 mV amplitude). Matched impedances without any discontinuities produce a response with a minimal amount of signal degradation. It is very common for interconnect interfaces to degrade the rise time of the pulse. A TDR examines how the rise time changes as the signal propagates through the interconnect from the source to the destination.

A TDR can provide an impedance waveform of the FPC interconnect as a function of distance. However the resolution is dependent on the electrical bandwidth of the fixturing. The fixturing may produce multiple reflections of the TDR pulse which may not allow the true impedance to be exhibited. Thus, the true impedance profile of the device under test may not be revealed by a TDR alone. A process to extract the appropriate waveforms from the TDR and eliminate the multiple reflections can allow the modeling of the true impedance of the device under test.

Because FPC interconnects are often used in differential signaling, the interconnect must be designed and tested as a differential system.

Differential Terminology

- **Differential System**
  - responds only to a potential difference between its balanced input terminals
  - suppresses outputs from common-mode voltages at its balanced input terminals
  - inputs must be balanced



2.2 Differential System

A differential system responds to a potential difference between the balanced input terminals. The minimum amount of input voltage required is reduced because the system is sensitive to the difference in the voltages of the output terminals. A differential system that depends on low voltage signaling, however, must be designed with a minimal amount of impedance discontinuities which cause an imbalance between two voltages.

Differential signaling applies two equal amplitude and opposite polarity voltages to the input terminals. For a FPC interconnect, two signal lines within a differential pair are in close proximity to each other and a conceptual understanding of coupling and impedance must be considered[4].

The Characteristic Impedance Matrix

$V_1 = Z_{11}I_1 + Z_{12}I_2$

$V_2 = Z_{22}I_2 + Z_{21}I_1$

Characteristic Impedance Matrix [ohms]:

	1	2
1	49.6	6.4
2	6.4	49.6

2.3 Characteristic Impedance Matrix

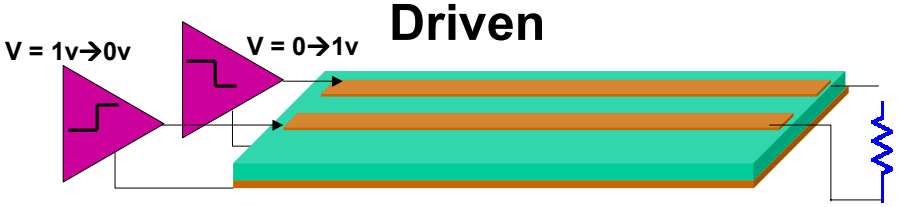
In a single-ended transmission line, the impedance is dependent upon the voltage across and the current flowing through the signal carrying conductor. With a differential transmission pair, the coupling factor between the two lines needs to be considered. If there were no coupling between two transmission lines, the impedance would be dependent on just the individual voltage and current line parameters. However, as soon as coupling is introduced, the voltage on one line is dependent on the current in an adjacent line. To explain these effects, the concept of impedance must be extended to allow for one trace interacting with another. This is handled by expanding the impedance into something called an Impedance Matrix.

Any two transmission lines, each with a signal path and a return path, can be modeled using an impedance matrix. The diagonal terms are the impedance of the line when there is no current in the adjacent line. This is sometimes called the self impedance. The off diagonal elements represent the amount of voltage noise induced on the adjacent trace when current flows on the active line. If there were little or no coupling, the off diagonal impedance would be near zero.

As the coupling between the lines increase, the off diagonal terms will increase. If microstrip traces were moved closer together, the diagonal impedance would not change very much, but the off diagonal terms would increase.

To obtain the characteristic impedance of the transmission lines, a differential mode and common mode TDR stimulus must be applied to the differential system.

The Impedance of One Line Depends on How the Other Is Driven



When both lines are driven with a differential signal, line 1 has an impedance of $Z_1 = Z_{odd}$:

$$Z_{odd} = (Z_{11} - Z_{12})$$

When both lines are driven with a common signal, line 1 has an impedance of $Z_1 = Z_{even}$:

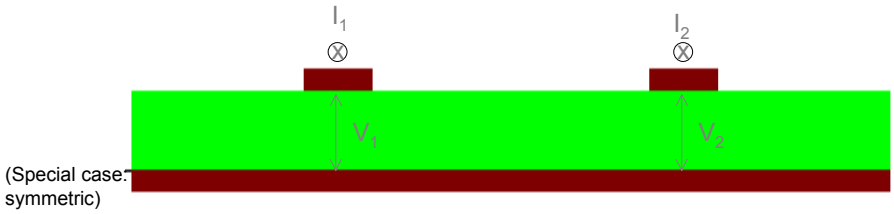
$$Z_{even} = (Z_{11} + Z_{12})$$

Dependence of Impedance on Driven Signals

When there is coupling between transmission lines, as in a differential pair, referring to the "impedance" of one line is ambiguous. The impedance will change depending on how the adjacent line is driven. When both lines are driven in common, the impedance of one line will be the even mode impedance. When both lines are driven differentially, the impedance of one line will be the odd mode impedance.

To measure the odd and even mode impedances requires applying simultaneous signals to each of the two lines. This requires using a dual channel TDR that can be configured for differential drive and common drive. With this instrument, the even and odd modes can be measured and the characteristic impedance matrix elements can be extracted.

Odd and Even Mode Impedance



$$V_{odd} = \frac{1}{2}(V_1 - V_2) \qquad Z_{odd} = \left.\frac{V_{odd}}{I_1}\right|_{V_{even}=0} \qquad Z_{odd} = (Z_{11} - Z_{12})$$

$$V_{even} = \frac{1}{2}(V_1 + V_2) \qquad Z_{even} = \left.\frac{V_{even}}{I_1}\right|_{V_{odd}=0} \qquad Z_{even} = (Z_{11} + Z_{12})$$

2.4 Odd and Even Modes

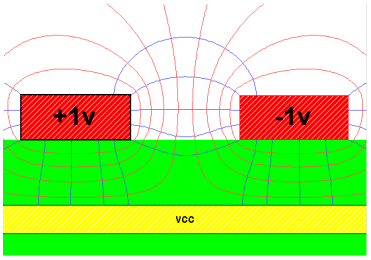
Definition of Odd and Even Mode Impedance

Based on the definition of the impedance matrix, and the definition of odd and even mode, the impedance of each mode can be calculated. The odd mode impedance is the impedance a driver would see, looking into one of the lines, when the pair of lines is driven in the odd mode, or with a differential signal. Likewise, the even mode impedance is the impedance a driver would see, looking into one of the lines, when the pair of lines is driven in the even mode, or by a common signal.

If there were no coupling, both the odd and even mode impedances would be equal, and equal to the impedance of just one isolated line. However, with coupling, there are additional current paths between the signal lines in odd mode, and the odd mode impedance decreases. Some current will flow not only from the first signal line to the return path, but through to the second signal line and then into the return path. This increased current through the coupling path results in a decrease in the odd mode impedance of one line with increasing coupling.

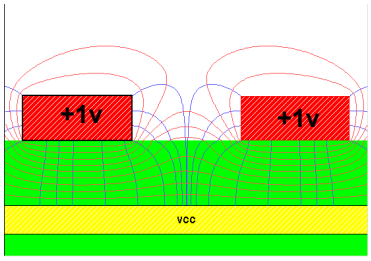
The even mode is also affected by the coupling. When driven with a common signal, there is no voltage difference between the two signal traces. There is thus no coupled current between the signal lines and the even mode impedance is higher than the odd mode.

Mode Pattern for Identical Traces*



Mode: odd, or 1, or a

Corresponds to differential driven



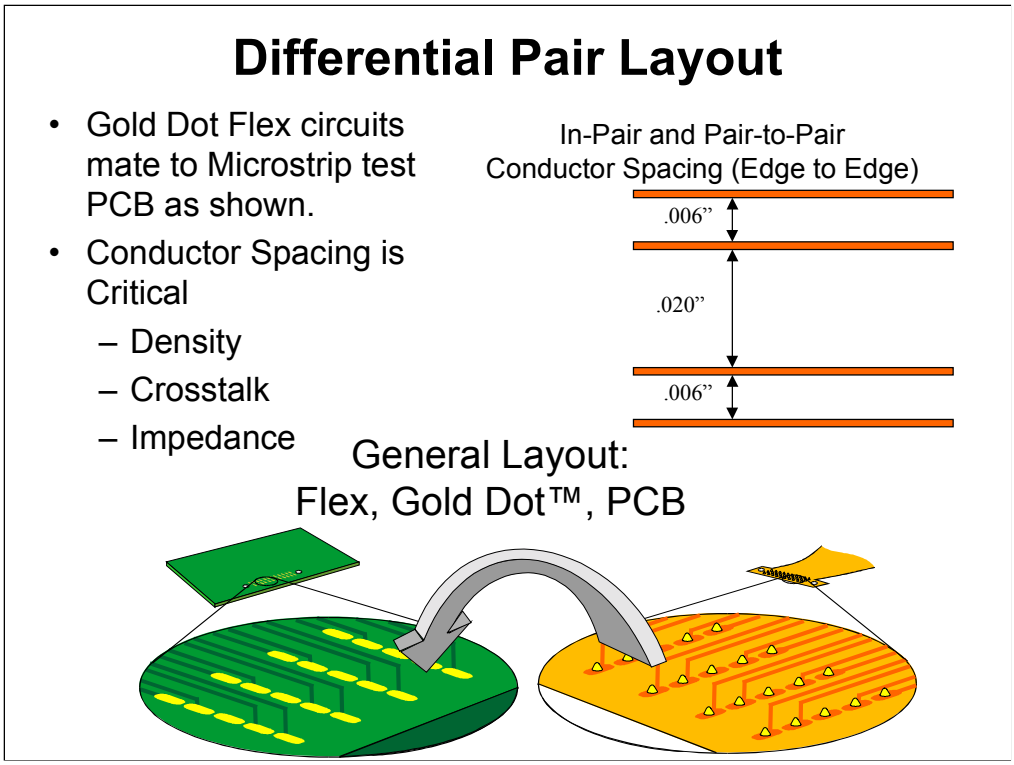
Mode: even, or 2, or b

Corresponds to common driven

*Simulation provided by Hyperlynx

Mode Pattern

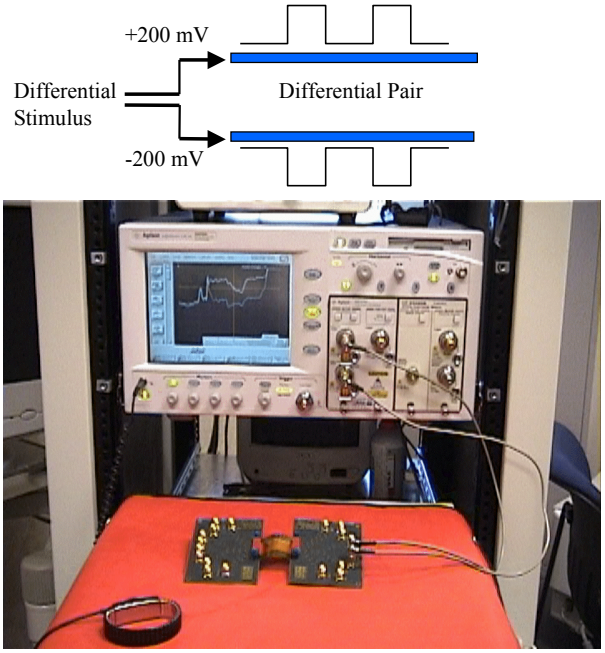
For a pair of transmission lines, any arbitrary voltage pattern may be imposed. However, certain patterns have special properties in that they will propagate down the line undistorted. These patterns are called modes. When the dielectric is inhomogeneous, and the conductors are identical, the mode patterns that propagate undistorted are the same voltage patterns as when driven differentially, with opposite edges or driven in common, with the same voltage edge polarity. We give these two modes the special names of odd and even modes.



2.5 Differential Pair Layout

For a differential pair FPC interconnect, adjacent pads on the PCB must be differentially and common mode driven to obtain the characteristic impedance. Once the stimulus is launched into the SMAs on the PCBs, the signals travel to pads at the edge of the PCB. The pads on the PCB are in contact with the FPC which contains Gold Dots at the same footprint as the PCB. The signals travel down differential pairs within the FPC until they reach the PCB on the other end of the FPC.

Setup for Impedance Measurements



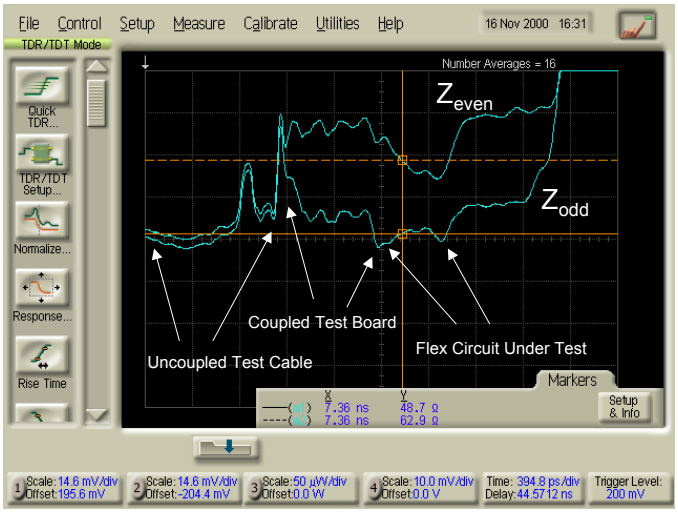
2.6 TDR Measurements

2.6.1 Impedance Measurements

The true impedance is obtained from the extraction of the even and odd mode impedance waveforms using TDR oscilloscope. Signals travel down adjacent lines within a differential pair. Though the signals are of the same amplitude, the polarity is the identical for even mode and opposite for odd mode. Using the even and odd mode impedance waveforms, the reference to ground waveform, and the measurement based simulation software, the true impedance of the device under test is computed.

Note the adequate attention to Electro-Static Discharge in the test laboratory. The use of a grounding strap, grounding mat and static gates on the TDR inputs will greatly enhance the protection of the test equipment.

Odd and Even Mode Impedance TDR Waveforms



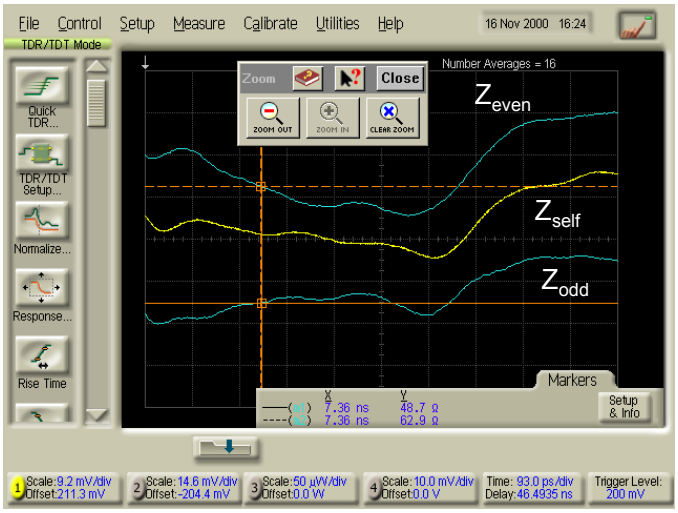
2.6.2 TDR Waveforms

Initial measurements of the jumper FPC interconnect using the TDR yielded an even mode impedance of 63 ohms and an odd mode impedance of 49 ohms. The even and odd mode impedance waveforms both display a slope in the waveform appearing as though Z_{even} and Z_{odd} change as a function of distance within the FPC interconnect.

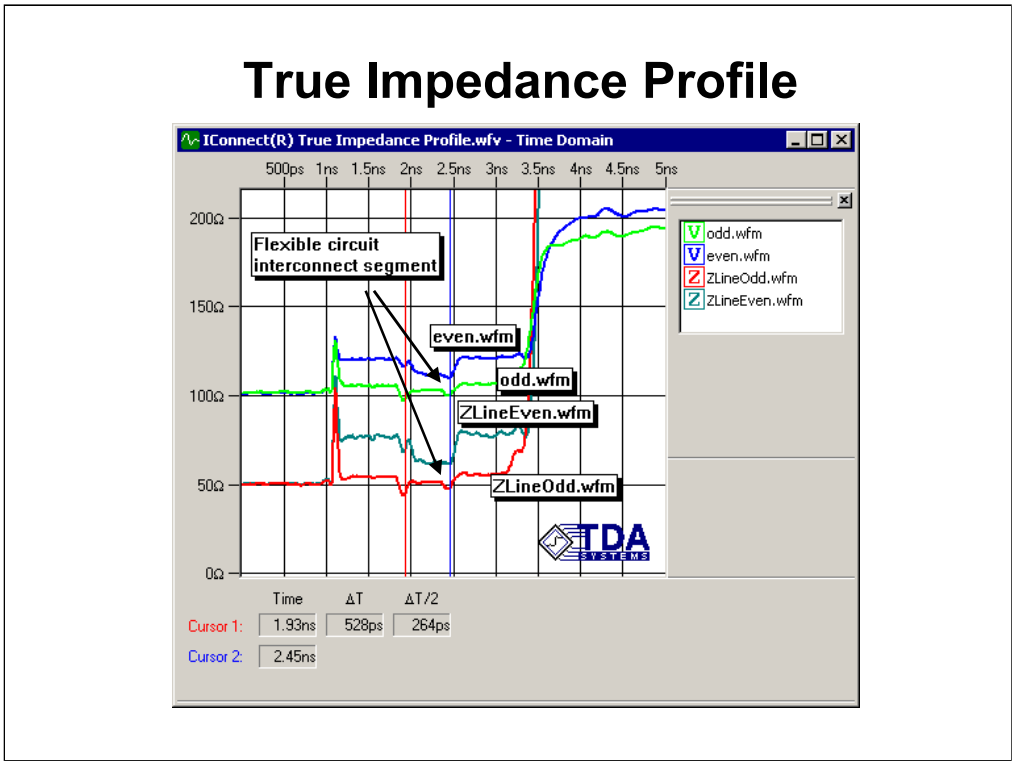
The test cables used to launch the stimuli into the PCB possess the same values for Z_{even} and Z_{odd} . One signal line within a differential pair will have $Z_{even} = Z_{odd}$ only if there is no coupling.

In our test case, coupling first occurs as the stimulus enters the SMA's soldered to the PCB. The separation of Z_{even} and Z_{odd} indicates that strong coupling is present. As the signals traverse the PCB to the FPC, the strong coupling continues. Coupling within two adjacent lines of the FPC continues and through the PCB to the other end of the FPC.

Zoom of Flex Circuit Under Test



A closer TDR screen capture of the Z_{even} and Z_{odd} reveals the coupling that occurs within the FPC, as illustrated by the separation of Z_{even} and Z_{odd} . A TDR measurement of Z_{self} (Z_{11}) is the impedance a line sees when driven alone. Without coupling from an adjacent line, this shows the relative effect of coupling yielding both Z_{even} and Z_{odd} . The $Z_{even} > Z_{odd}$ assists in increasing common mode noise rejection, a characteristic important to designing a differential system.

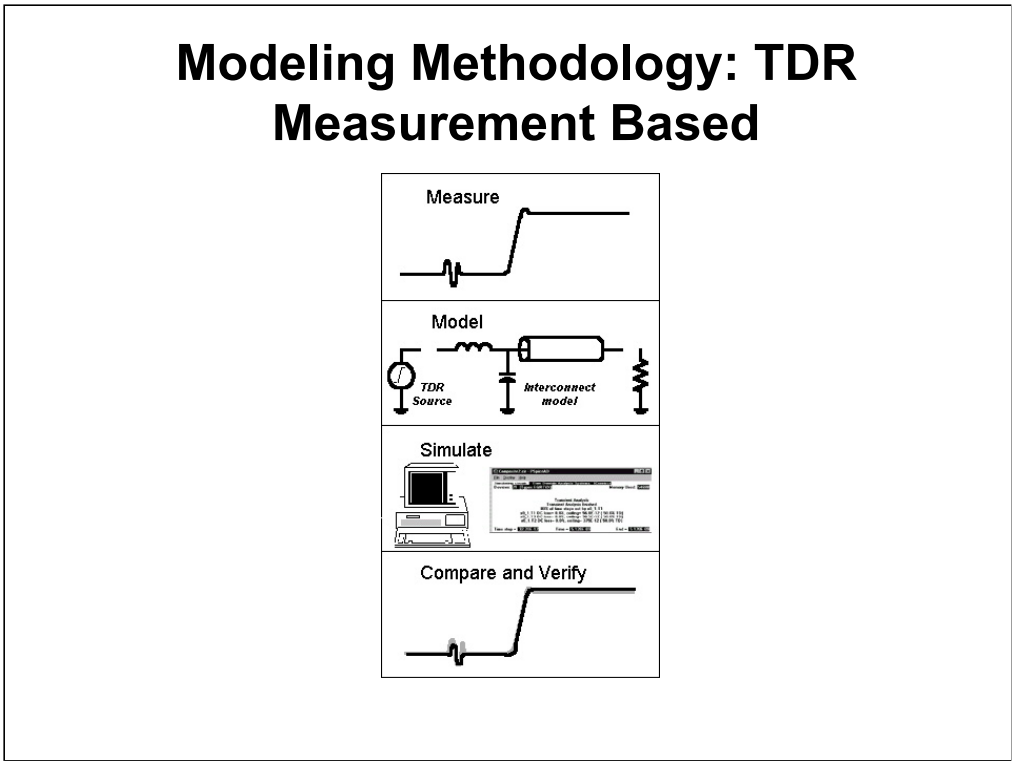


2.6.2 True Impedance Profile

One phenomena that all TDR instruments exhibit is the multiple reflections effect. The true impedance profile algorithm implemented in the software, coupled to the TDR oscilloscope via GPIB, allows the designer to remove these multiple reflections and obtain the true signature of the device under test[5].

On close examination of both even and odd TDR waveforms, it appears that there is some upward slope in the waveform due to the losses in the flex interconnect. In reality, this slope is mostly due to multiple reflections in the TDR waveform, as the true impedance profile waveform computed in the software clearly shows.

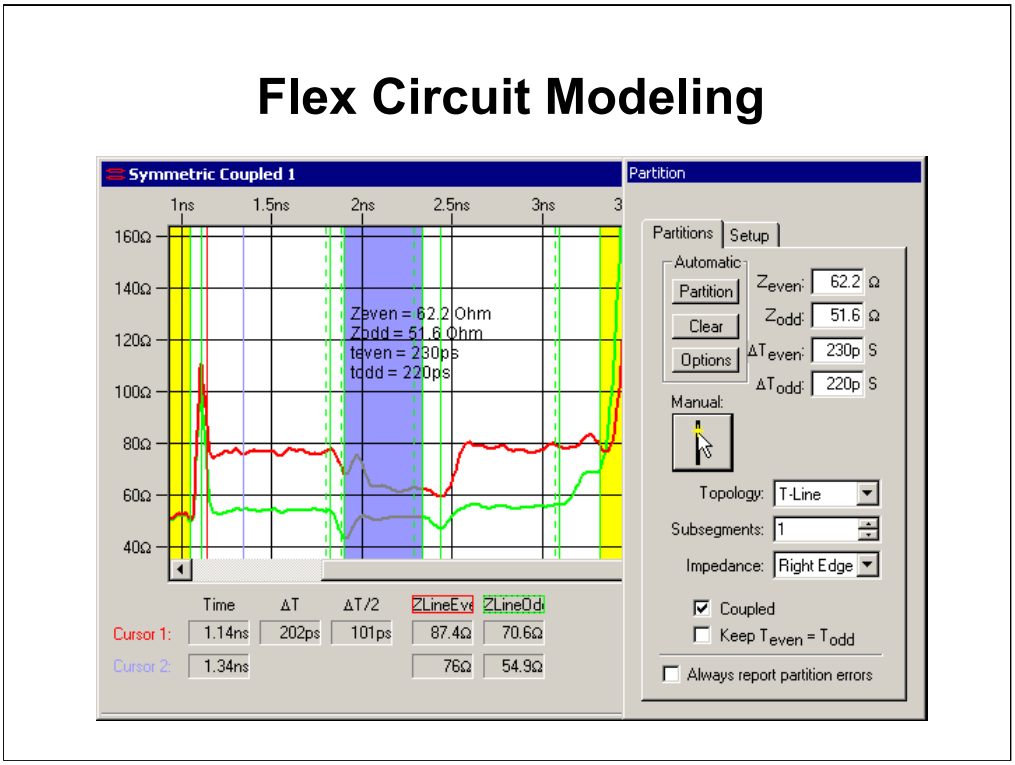
The true characteristic impedance of the flexible circuit interconnect based on measurement based simulation software does not include the multiple reflections inherent in the TDR waveform measurement. Elimination of multiple reflections allows clear identification of excess inductance and capacitance at interfaces as well as coupling present in each component. These two enhancements assist in revealing what is commonly called the true impedance profile of interconnect components.



2.7 Measurement-Based Simulation

The measurement-based approach described here employs the Measure-Model-Verify philosophy. A prototype is measured using TDR techniques, and based on the acquired data, an equivalent circuit model is created. The model is verified through simulation, with the same excitation and termination used for simulation and measurement. The simulated and measured waveforms are then compared and the model is verified and adjusted if necessary.

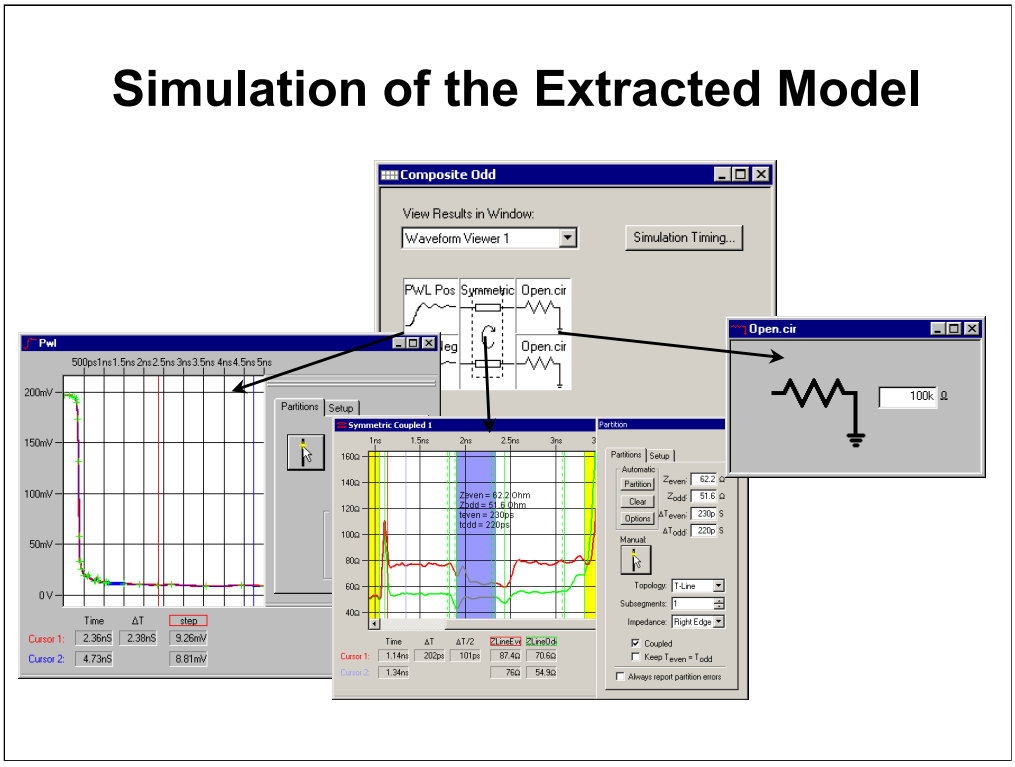
This measurement-based approach does not contradict with the design approach that utilizes analytical tools, such as electromagnetic field solvers. If the component design was based on an electromagnetic field solver analysis, a prototype must still be fabricated. At this point, the prototype must be carefully characterized and accurate models for the prototype generated. The Measure-Model-Verify approach, again in this case, can be used in order to ease the modeling work and create an accurate prototype model from measurements. If the measurement-based model differs from the original analytical model, then the difference between assumptions in the field solver and the measurement reality must be reconciled and the model representing the prototype, as it will be used in the actual system, must be defined.



2.7.1 Flexible Circuit Modeling

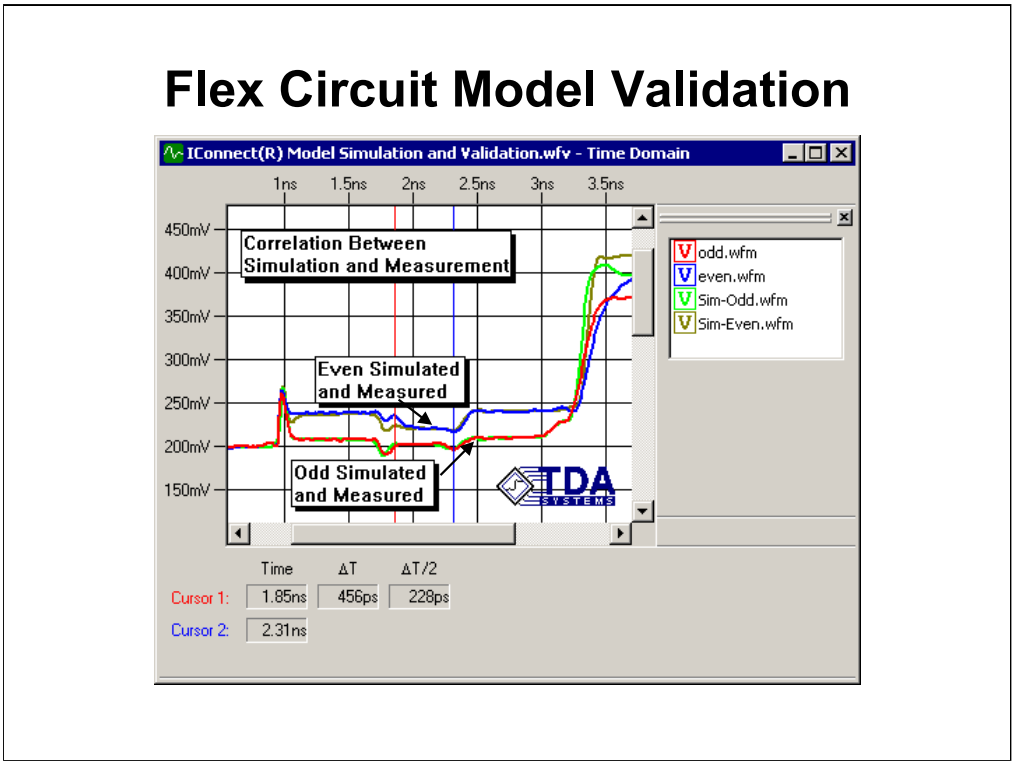
For single line modeling, the impedance profile waveform is partitioned and appropriate circuit topologies are selected for each partition[6]. The segments of constant impedance are evidently the transmission lines on the board, whereas the dips and peaks in the waveform are the capacitive and inductive discontinuities. On the true impedance profile waveform, the board designer can zoom in on the part of the DUT that needs to be modeled, without running the risk of having multiple reflection effects distort the impedance of the DUT in that section of the trace. Unessential information, such as reflections at the connector-to-board interface, can be windowed out during the modeling session. Once the engineer has segmented the impedance profile waveform, the software automatically computes the impedances and propagation delays for the lines on the board and values for capacitive and inductive discontinuities.

The odd and even mode impedances are now isolated from reflections not relevant to differential signaling. These two impedance waveforms and their values are easily extracted from the measurement based impedance profiles. The odd mode impedance can now be used to optimize the design of the FPC interconnect for differential signaling.



2.7.2 Simulation of the Extracted Model

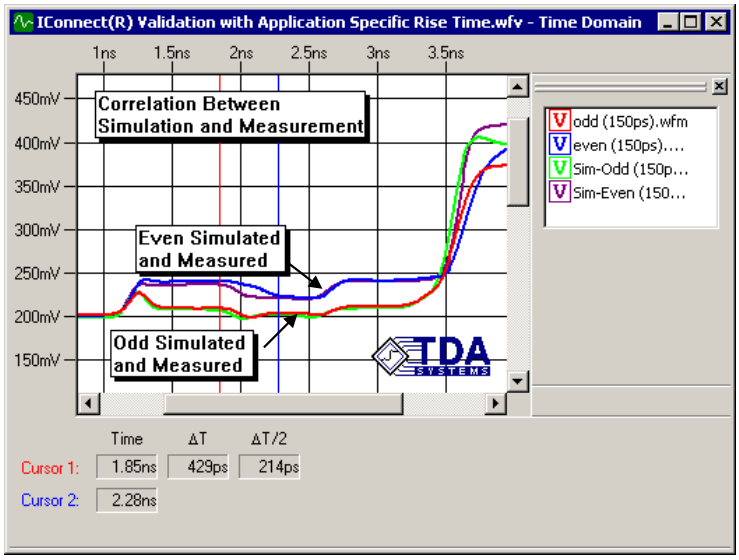
The model can then be verified using an integrated interface to SPICE. The extracted model is complemented with a piece-wise linear source that should accurately represent the TDR oscilloscope incident step waveform during the simulation, and the same termination as the one used during the measurement.



2.7.3 Flex Circuit Modeling Validation

To verify the created model, a designer needs to create a composite model in the software. The composite model complements the extracted DUT model with the source and termination that emulate the TDR measurement source and termination. Using an integrated interface to a SPICE simulator, the designer can simulate this composite model, and based on the resulting simulation waveforms, verify the accuracy of the DUT model. Both even and odd mode stimuli must be used in simulations in order to ensure that the model accurately predicts both even and odd modes of signal propagation. One can see that with the exception of the SMA connectors, which are not part of the differential line, the model accurately predicts the signal propagation. In addition, the connectors can be modeled using lumped circuit modeling capability in the software.

Using Rise Time Filtering to Achieve Simple Models



Rise Time Filtering

A model must be no more complex than is necessary to represent the DUT accurately at the given system rise time or analog bandwidth. Examining the relationship between the rise time of a TDR oscilloscope and the rise time of a DUT, a typical TDR system rise time is quite fast, on the order of 30-40 ps. On the other hand, even today's rise times of signals on the circuit board rarely reach 100 ps, and more often are on the order of 500 ps to 1 ns.

With faster TDR system rise times, the DUT traces may exhibit losses that are not present under normal operating conditions for the DUT. In addition, the impedance that the lumped discontinuities present to the test signal is dependent to the highest frequency present in the test signal bandwidth, as described by equations

$$Z = 1 / (j\ 2\pi fC) \qquad Z = j\ 2\pi fL$$

At faster rise times, the capacitive discontinuity will present a deeper "dip", whereas an inductive discontinuity will be a present a larger "spike" in relation to the impedance of the transmission lines surrounding the discontinuity. Consequently, the impedance discontinuity ΔZ in the DUT will be larger for a faster rise time, which may not accurately represent the impedance value at the DUT operating rise time.

At the typical TDR oscilloscope rise time of about 40 ps, the correlation between the measurement and simulation of the given model is good, but not perfect. However, once both waveforms are filtered to about 150 ps equivalent rise time, the discrepancies between the model simulations and measurements become negligible. The resulting model will represent the

S-Parameters from TDR

- Conversion from TDR to S-parameters:

$$S(f) = FFT(\rho(t))$$

  - S11 (return loss) TDR on Channel 1
  - S11 (return loss) TDR on Channel 2
  - S21 (insertion loss) TDT from Channel 1 to Channel 2
  - S12 (insertion loss) TDT from Channel 1 to Channel 2
- Accuracy comparable to 10 GHz VNAs
  - Use Agilent normalization for best accuracy
  - Increase # of averages for better dynamic range

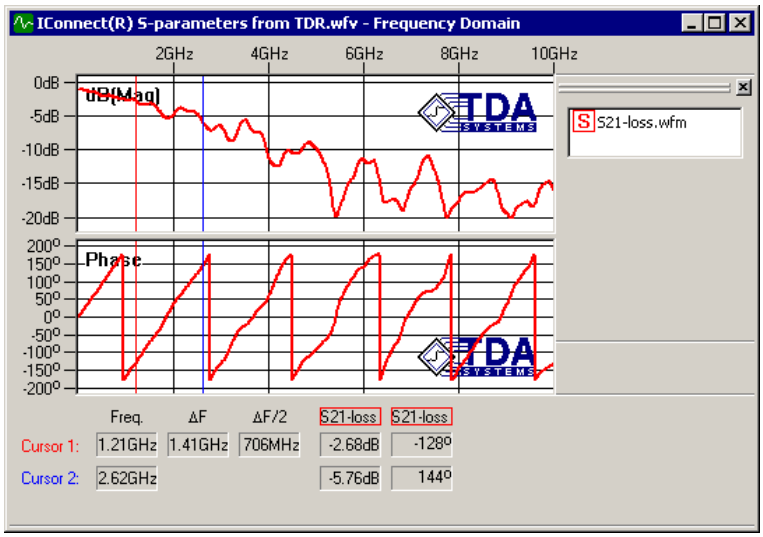
2.7.4 S-Parameters from TDR

It is generally believed that TDR and network analyzers are completely different instruments. However, reality is that there is such a thing as time domain option for most network analyzers. It is now possible to easily compute S-parameters from TDR measurements. TDR measurement on channel 1 will give the designer S11 and TDR measurement on channel 2 will give the designer S22. Similarly TDT (Time Domain Transmission) can provide the designer with S21 (channel 1 stimulus, channel 2 TDT response) and S12 (channel 2 stimulus, channel 1 TDT response). The computational procedure of S-parameters from TDR measurements involves FFT (Fast Fourier Transform) and appropriate windowing for the time domain waveform.

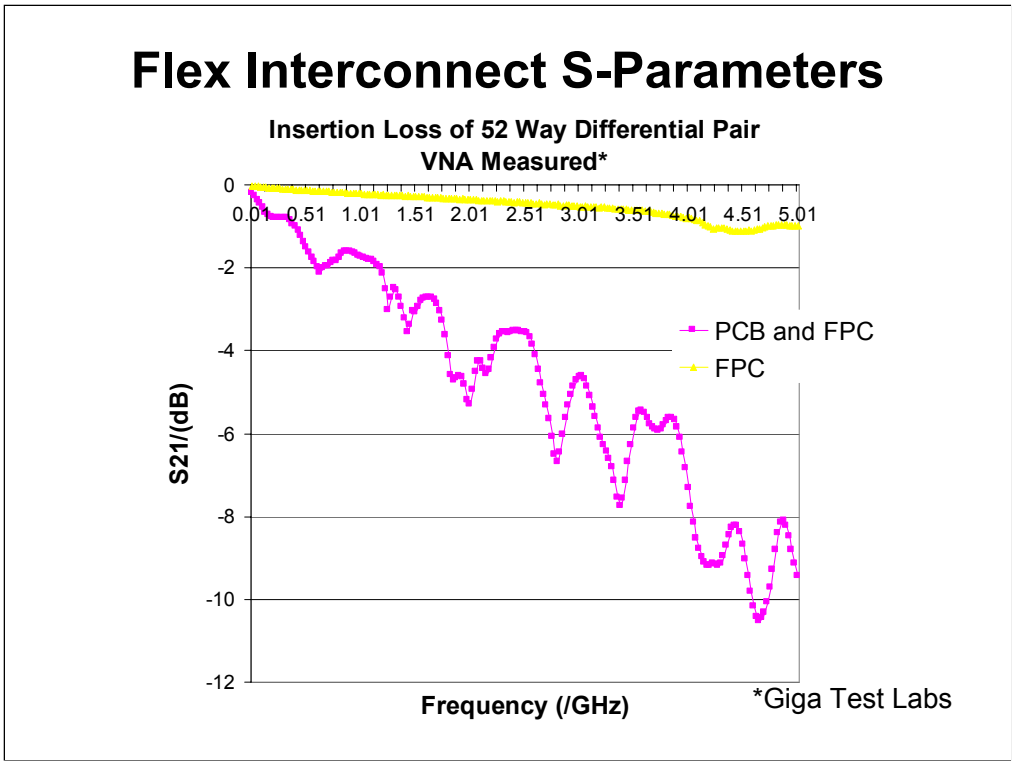
The accuracy of the S-parameter computation completely depends on the accuracy of the TDR measurement. A TDR oscilloscope normalization is conceptually similar to the frequency domain calibration of VNAs. If the TDR normalization algorithm resident within the Agilent TDR oscilloscope is used, S-parameters of accuracy comparable to that of a 10 GHz network analyzer can be easily achieved. In addition, increasing the number of averages in time domain 2 times results in 3dB improvement in dynamic range [7].

It must be noted that the frequency step f_{step} of the S-parameters computed from TDR is completely determined by the length of the time domain window t_d, i.e. $f_{step} = 1 / t_d$. At times, padding or interpolation may be required to obtain a smooth S-parameter curve.

Flex Interconnect S-Parameters



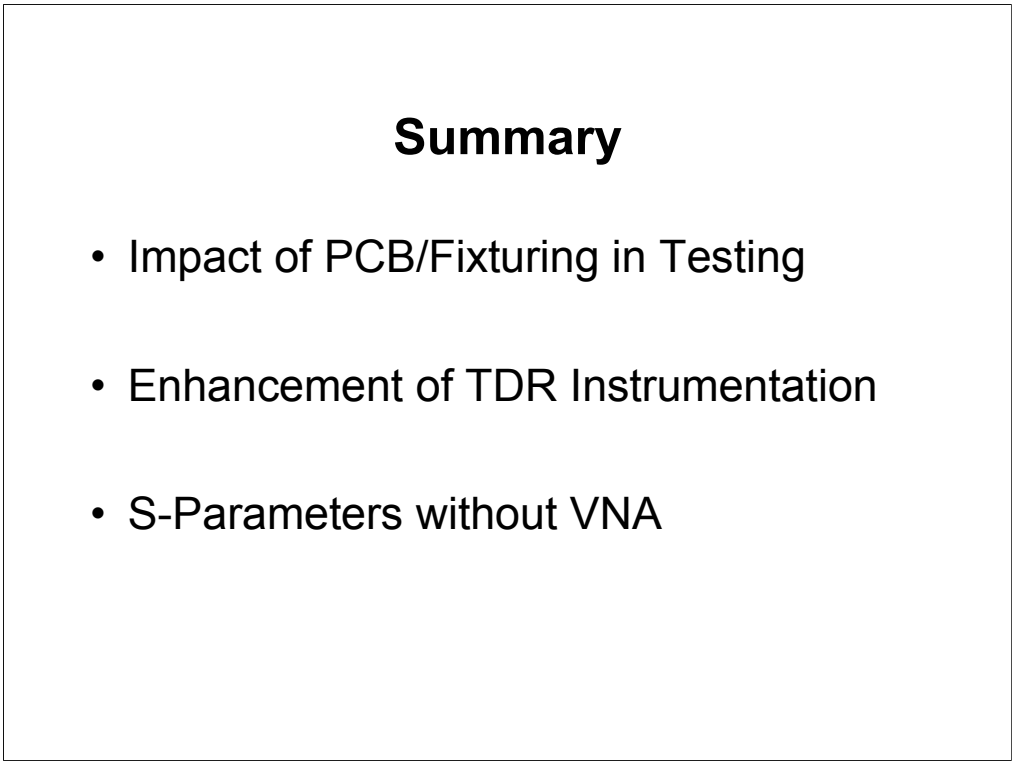
S-parameters for the flex circuit were obtained using TDT data of the circuit. This insertion loss (S21) graph is dominated, however, by the loss in the DUT interface boards and reflections between the interface boards and the DUT.



2.8 Compare and Verify Measurements

S-parameters were measured using VNA for both the Gold Dot FPC interconnect (PCB and FPC) as well as the Gold Dot FPC alone. The Gold Dot FPC interconnect demonstrated a bandwidth of approximately 1.4 GHz. This correlates with the bandwidth produced by the software of approximately 1.5 GHz. These measurements agree well up to 5 GHz, where both the simulation and the VNA measurements demonstrate an insertion loss of approximately 10 dB. It should be noted that without performing measurements on each component separately, this bandwidth measurement on the VNA cannot easily identify the location of the insertion loss within the FPC interconnect.

An additional VNA measurement was performed on the Gold Dot FPC alone. The VNA measurement on the Gold Dot FPC demonstrated approximately 1dB of loss up to 5 GHz. This clearly shows that the VNA measured bandwidth of the Gold Dot FPC interconnect is masked by the bandwidth of the PCBs. On the other hand, the proposed method of characterization and modeling of an FPC interconnect can clearly identify the components and interfaces contributing to signal degradation. This due to the TDR's ability to display the spatial relationship of impedance to interconnect component.



3.0 Summary

Although this method was demonstrated on Gold Dot FPC interconnects, it can also be applied to high-speed interconnects possessing a variety of components. This method of characterizing differential FPC interconnects allows the design engineer to isolate and identify traits in the physical layer of high-speed systems. TDR waveforms show the intuitive spatial relationship between impedance and the physical geometry of hardware. This gives insight into both the test fixturing and the device under test, thus yielding better understanding of the complete system.

The analysis of both even and odd mode signal propagation is critical to differential circuit design. Measuring the separation of the even and odd impedance gives the designer an indication of the degree of coupling between a differential pair. Partitioning the odd mode impedance waveform of the interconnect components can be used to design smooth transitions.

Today's high speed digital signals present many challenges to the design engineer. Maintaining signal integrity in differential circuitry will require the engineer to become familiar with many new tools. The insight brought about by these tools used in the laboratory will help the designer achieve a controlled impedance environment. This will ultimately enable a faster risetime signal to transmit through the physical layer, thus allowing data rates to expand at a feverish pace.

References

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[5]D.Smolyansky, S.Corey, “PCB Interconnect Characterization from TDR Measurements”-TDA Systems Application Note PCBD-0699-0, published in Printed Circuit Design Magazine, May 1999.

[6]D.Smolyansky, S.Corey, “Characterization of Differential Interconnects from TDR Measurements-TDA Systems Application Note DIFF-1199, published in Microwave Journal, March 2000.

[7]S.Diamond, S.Pepper, "Decode Dynamic Range in Time/Frequency□Domain Analyzers", Microwaves & RF, September 1993, p. 102-110.

4.0 Resources

4.1 Equipment

Agilent Technologies 86100A Digital Communications Analyzer (DCA)

Agilent Technologies 54754A Time Domain Reflectometry (TDR) Plug-Module

Agilent Technologies 83480A Digital Communications Analyzer (DCA)

4.2 Services

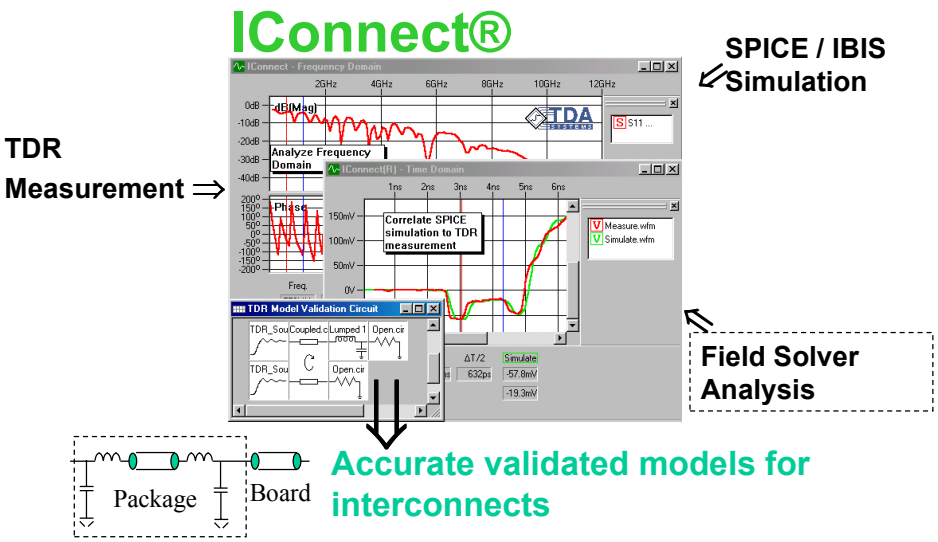
IConnect, TDA Systems

Giga Test Labs

Resources

- Agilent www.agilent.com/comms/tdr
- TDA Systems www.tdasystems.com
- Packard Hughes www.golddot.com
- Bogatin Enterprises www.bogent.com

IConnect® TDR Software



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